Quasi-Digital Low-Dropout Voltage Regulator uses Controlled Pass Transistors

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***Abstract*— This article presents a low quiescent current output-capacitorless quasi-digital CMOS LDO regulator with controlled pass transistors according to load demands. The pass transistor of the LDO is broken up to two smaller sizes based on a breakup criterion defined here, which considers the maximum output voltage variations to different load current steps to find the suitable current boundary for breaking up. This criterion shows that low load conditions will cause more output variations and settling time if the pass transistor is used in its maximum size. Therefore, using one smaller transistor for low load currents, and another one larger for higher currents, is the best trade-off between output variations, complexity, and power dissipation. The proposed LDO regulator has been designed and post-simulated in HSPICE in a 0.35 μm CMOS process to supply a load current between 0-100 mA while consumes 7.6 μA quiescent current. The results reveal 46% and 69% improvement on the output voltage variations and settling time, respectively.**

I. INTRODUCTION

Nowadays, power management is a very important issue in battery supplied electronic devices. Advanced power management units for system on chip (SoC) applications need multiple voltage regulators to drive various operational blocks [1], [2]. Usually, low-dropout (LDO) voltage regulators are a part of these power management units which have less output ripple in comparison with switching ones. However, in general, they suffer from lower efficiency. The typical structure of a LDO consists of an error amplifier, a pass transistor controlled by the aforementioned error amplifier, a feedback network, and an output capacitor. Most of conventional LDOs use a large off-chip capacitor for stability requirements which cannot be implemented as on-chip capacitors, leading to need output-capacitorless LDOs for SoC applications [3].

Some papers in connection with output-capacitorless LDOs have been reported in recent years [4-9]. In this way, the reported LDO in [4] uses a capacitor multiplier stage as a separate one to improve the dynamic performance of the LDO, while increases its power consumption. The LDOs in [5] and [6] have simple structure based on the flipped voltage follower (FVF). However, they suffer from weak load and line regulations. In [7], the proposal of an ultra fast transient response LDO has the problem of high consumption and significant high quiescent current. Thus, it is not appropriate for low power applications and battery-based devices. The LDO in [8] uses a pole-zero tracking frequency compensation technique in which an "adaptive" zero created thanks to a variable linear resistance cancels the regulator output pole. However, mismatch can degrade the compensation strategy. Finally, Nested-Miller compensation technique with a programmable capacitor array was used in [9] in order to provide good phase margin and control the damping factor. Nevertheless, the output voltage of LDO changes dramatically when the load current changes.

In addition, recently, some digital LDOs with off-chip output capacitor have been reported. The LDO in [10] can deliver only 200 μA current to the load while consumes 2.7 μA quiescent current and has one array of 256 power transistors. On the other hand, [11] shows a digitally controlled LDO regulator in which the output voltage variation and settling time to the load transient is quite large, 700 mV and 1.77 ms, respectively. The quiescent current of the LDO in [12] is 164.5 μA, which can discharge fast the battery voltage.

In typical LDO circuits, a very large size pass transistor is used to support the low dropout performance and high current demanding loads. This involves that a large capacitance will be created at the gate of pass transistor, making a limit on slew-rate at this node. Additionally, since the charge and discharge process of such a large capacitor takes a long time, the feedback loop reaction against fast load variations will be slow, destroying feedback loop response of the circuit. Such a large size device is designed for maximum load current. However, this maximum current is not needed for all times, since the LDO is in standby mode in most of the time [8]. Therefore, it can be possible to break up the pass transistor to smaller sizes and control their performance according to the load demands. This paper presents an output-capacitorless LDO in which the control of the pass transistor sizes is carried out in a quasi-digital manner. Section II describes the pass transistor breakup criterion to smaller sizes. The proposed LDO architecture is presented in section III. Finally, circuit characterization and conclusion are in sections IV and V, respectively.

II. PASS TRANSISTOR BREAKUP CRITERION

As mentioned before, using a large pass transistor creates a large capacitance at its gate terminal, which takes a long

time to charge and discharge. Therefore, the output voltage variations to load current and/or input voltage transients will be increased; that is, the transient load and lines regulations get worse. Regarding load transient response, a breakup criterion (BC, expressed in *mV*/*mA*) is defined here, as Eq. (1), by evaluating the maximum output voltage variations to different load current variation steps for the maximum size power transistor in order to find a suitable load current boundary for breaking up the large pass transistor into smaller ones.

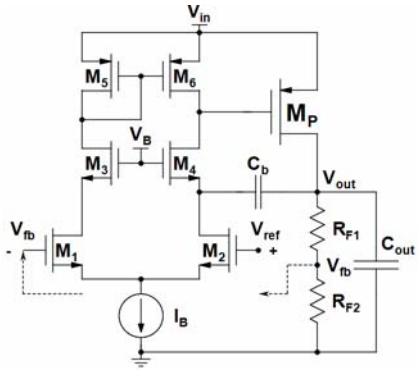
$$BC = \frac{\text{Maximum Ouput Voltage Variations}}{\text{Load Current Variations}} \qquad (1)$$

It should be mentioned that each pass transistor needs its own control circuitry, adding more power dissipation and complexity. As a consequence, a trade-off should be considered between number of pass transistors, power consumption, and complexity. Fig. 1(*a*) shows a simple LDO regulator, which consists of a cascode error amplifier with a current buffer-based compensation scheme, a pass transistor, and feedback network. Fig. 1(*b*) shows the defined BC versus different load current steps for the LDO shown in Fig. 1(*a*). As it can be seen, the maximum output voltage variation occurs at low load conditions (less than 1 *mA*). Therefore, this current range is selected as a boundary for breaking up the pass transistor, and one transistor is utilized to cover this current range. Additionally, with regards to Fig. 1(*a*), other steps of load current variations cause less variations at the output voltage and so higher load currents can be covered by another pass transistor. Consequently, the designed LDO regulator will have two pass transistors while second one turns on when the load current is higher than 1 *mA*.

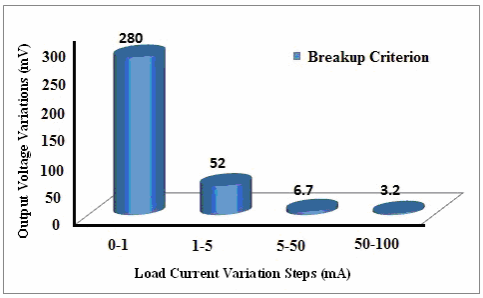
III. The Proposed LDO Architecture

Fig. 2 shows the transistor level schematic of the proposed LDO. Transistors M_1–M_6 make the cascode error amplifier. Capacitor C_b and transistor M_4 form a current buffer for frequency compensation. R_{f1} and R_{f2} are the feedback network resistors and C_{out} is the output capacitor. In order to achieve high current efficiency, especially at low load currents, the proposed LDO is designed with a small bias current I_b, and extra bias currents for higher loads are provided through a dynamic biasing approach by transistor M_7 and load current sampling network M_8–M_9. Transistors M_{P1} and M_{P2} are as pass transistors and responsible for delivering currents to the load. Transistor M_{P1}, with the size of 50 µ*m*/0.35 µ*m*, is used for low load current steps (less than 1 *mA*, according to the BC obtained in previous section) and M_{P2}, with the size of 3500 µ*m*/0.35 µ*m*, provides the current for loads higher than 1 *mA*. Transistors M_{12} and M_{13} act as a level shifter to provide a suitable control signal from the error amplifier to the pass transistor M_{P2}. Finally, transistors M_{10} and M_{11} control the second pass transistor gate voltage with respect to the output load current.

The mechanism of voltage regulation is discussed in the following. In case that the load current increases, the output voltage is prone to drop. Thus, the gate-source voltage of M_1 decreases. As a result, the drain current of M_1, M_3, M_5, and M_6 will be decreased, and that of M_2 and M_4 will be increased causing the gate voltage of M_{P1} to decrease and more current will source to the load. When the load current achieves more than the boundary, the gate voltage of M_{10} and M_{11} will be increased through the load current sampling network (transistors M_8–M_9) and, therefore, their drain voltage drops turning on the second pass transistor M_{P2} to deliver more current to the load. The higher the load current is, the lower the drain voltage of M_{10} and M_{11} is, and as a result, the sufficient current will be deliver to the load through M_{P2}. In no-load condition, M_{10} is in triode and M_{11} is cut-off. In full-load condition, both transistors are in saturation. An analogous mechanism occurs when the load current decreases.



(*a*)



(*b*)

Figure 1. (*a*) Circuit schematic of the simple LDO voltage regulator. (*b*) Breakup criterion (BC) for the LDO of Fig. 1(*a*).

Fig. 3 shows the small signal model of the proposed LDO regulator in which R_1 and C_1 are the output resistance and equivalent capacitance at the output node of error amplifier, respectively. R_{out} is the output resistance of the LDO which equals $R_{o2} = r_{o,M_{p1}} \| (R_{f1} + R_{f2}) \| R_{Load}$ for load currents lower than the boarder line (1 *mA*, in the considered case), and equals $R_{o3} = r_{o,M_{p1}} \| r_{o,M_{p2}} \| (R_{f1} + R_{f2}) \| R_{Load}$ for load currents more than that. Additionally, when the load current is lower than the boarder line, the dashed line part will not operate, and, for load currents more than that, this part will be added to the circuit and the pass transistor size will be increased. If the level shifter (buffer) stage is designed carefully so that its output pole is crated at higher frequencies, this stage can be ignored for small signal analysis and, hence, for higher load currents, the effective transconductance of pass transistors are sum of the g_{mp1} and g_{mp2} which approximately equals g_{mp2} (notice that g_{mp2} is much greater than g_{mp1}). Carrying out small signal analysis on the circuit, the transfer function is shown in Eq. (2).

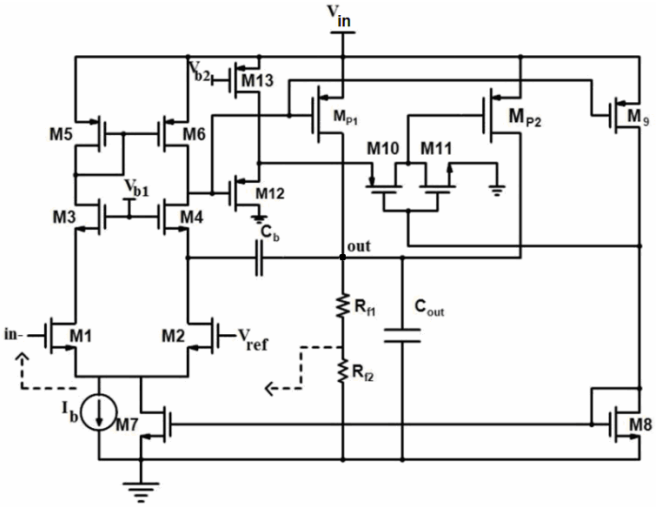


Figure 2. Schematic of the proposed LDO.

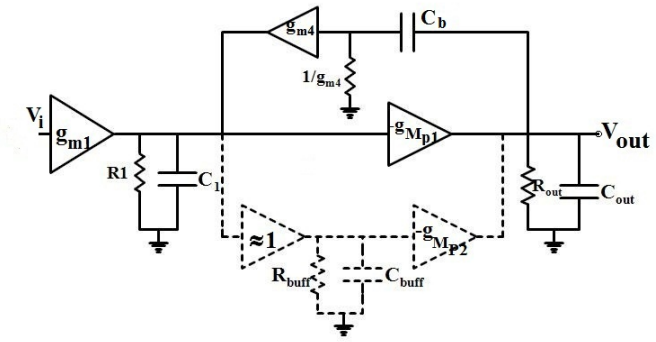


Figure 3. Small signal model of the proposed LDO.

$$A_V = \frac{-\beta A_0 (1-\frac{s}{Z_1})}{(1-\frac{s}{P_1})(1-\frac{s}{P_2})(1-\frac{s}{P_3})}, \qquad (2)$$

where, the feedback factor, DC gain, pole-zero positions, and unity-gain frequency are as following:

$$A_0 = g_{m1} g_{mp} R_1 R_{out} \qquad \beta = \frac{R_{f2}}{R_{f1}+R_{f2}} \qquad (3)$$

$$P_1 = -\frac{1}{g_{mp} C_b R_1 R_{out}} \qquad Z_1 = -\frac{g_{m4}}{C_b} \qquad (4)$$

$$P_2 \approx -\frac{C_b g_{mp}}{C_1 C_{out}} \qquad P_3 \approx -\frac{g_{m4}}{C_b} \qquad (5)$$

$$\omega_T = \frac{g_{m1}}{C_b} \qquad (6)$$

For load currents lower than the boundary, g_{mp1} and R_{o2} are represented, respectively, by g_{mp} and R_{out} in Eqs. (3)–(6), while g_{mp2} and R_{o3} are represented for higher load currents. As it is obvious, the pole P_3 and the zero Z_1 can cancel each other. In addition, the pole P_2 moves to higher frequencies by a factor of C_b/C_1, which guarantees the LDO stability.

Fig. 4 shows the open loop frequency response of the proposed LDO regulator with C_b=2 *pF* and C_{out}=100 *pF*. As it can be seen, the LDO is stable over the entire load current range, and the phase margins for no-load and full-load conditions are 91º and 66º, respectively. Additionally, the effect of process variation (slow-slow and fast-fast) on the frequency response was checked which indicates that the LDO has less sensitivity to the process variations.

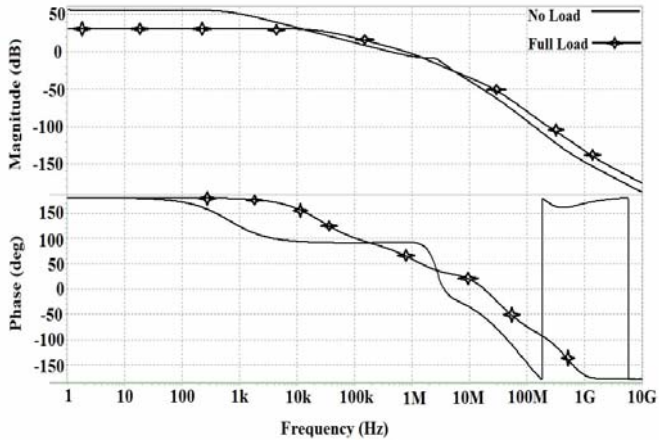


Figure 4. Open loop frequency response of the proposed LDO for no-load and full-load conditions.

IV. Circuit Characterization

The proposed LDO topology has been designed to source a load current between 0-100 *mA* and the obtained results correspond to HSPICE post simulations in a 0.35 µ*m* CMOS process. The dropout voltage of the LDO was set to 200 *mV* for 3–3.5 *V* input voltage. The total quiescent current of the LDO at no-load and full-load conditions are 7.6 and 50 µA, respectively. The power supply ripple rejection (PSR) of the LDO at 10 *kHz* frequency is –57 and –44 *dB* under no-load and full-load conditions, respectively. In addition, the load and line regulations are 0.23 *mV*/*mA* and 1.5 *mV*/*V*, respectively.

Fig. 5 shows the output voltage transient response of the LDO for different load current changes with rise and fall times of 1 µs. As it is obvious, the maximum output voltage deviation from its desired value is 270 *mV* which occurs at 20 µs with duration of only 1.1 µs. Line transient response of the LDO is shown in Fig. 6, in which the line voltage changes between 3 *V* and 3.5 *V* with rise and fall times of 1 µs. It demonstrates that the maximum output variation is only 12 *mV* and its settling time is 2 µs.

Table I provides a performance comparison between the proposed LDO and recent works. In order to have a fair and coherent comparison, other LDOs except [12] are simulated in HSPICE and the table results correspond to their simulations. The results of the proposed LDO without controlling the pass transistor are also included. As it can be seen, both the output voltage variation and settling time will be increased without controlling the pass transistor. The figure of merit ($FOM = \Delta V_{out} C_{out} I_Q / I^2_{out,\max}$) used in [7] is

adopted here to compare the transient response of different LDOs. Notice that smaller FOM shows better transient operation. As it can be seen, controlling the power transistor size with regards to the load current, leads to better transient LDO performance.

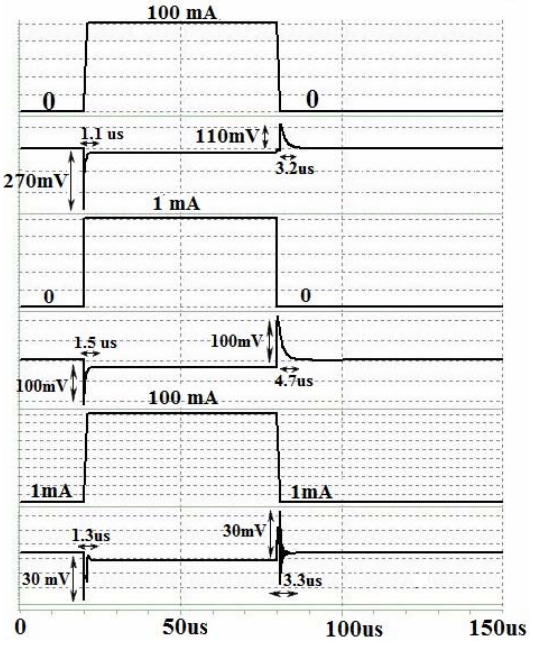


Figure 5. Load transient response of the proposed LDO.

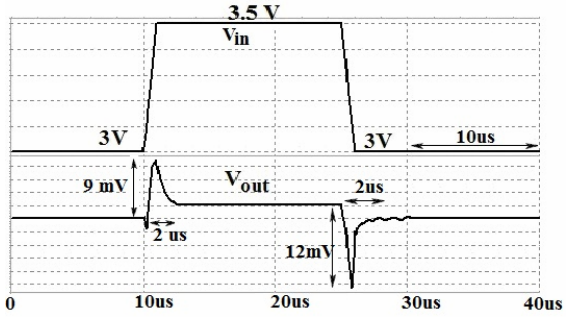


Figure 6. Line transient response of the proposed LDO.

TABLE I. PERFORMANCE COMPARISON

Parameters	[5]	[9]	[11]	[12]	This Work	
					Without Control	With Control
Tech (µm)	0.35	0.35	0.35	65 nm	0.35	0.35
V_{in} (V)	1.2	2	0.9	1.1	3	3
V_{out} (V)	1	1.8	0.7	0.5-1	2.8	2.8
I_{out} (mA)	0-50	0-150	0-50	0-100	0-100	0-100
I_Q (µA)	95	20	4.7	164.5	6	7.6
C_{out} (pF)	20	100	100	4.5 nF off-chip	100	100
T_{settle} (µs)	1.4	90>	1.77 ms	N.A.	16	≈4.7
ΔV_{out} (mV)	200	540	700	120	500	270
CE (%)	99.8	99.9	99.9	99.8	99.9	99.9
FOM (fs)	152	48	131.6	8883	30	20.52

V. CONCLUSION

This paper presents an output-capacitorless quasi-digital CMOS LDO regulator. The pass transistor of the LDO is broken up to two smaller sizes, one for low currents and another one for high currents, based on a breakup criterion which considers the maximum output voltage variations to different load current steps. Post-layout simulation results in a 0.35 µm CMOS process show 46% and 69% improvement on the output voltage variations and settling time, respectively, in comparison with the case that the power transistor is used in its maximum size.

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